REMARKS

Claims 1-23 are pending in the application. Claims 1, 13, 22, and 23 are the independent claims. In an office action dated 12/08/05, claims 1-23 were rejected as anticipated by U.S. Pat. 6,327,614 (Asano) in view of U.S. Pat. App. 2004/0024941 (Olarig). Claim 23 has been amended to clearly state that the adaptable cache provided therein comprises a data interface, a core logic, and electronic storage media. The rejection is respectfully traversed.

Claims 1-23 were rejected under 35 U.S.C § 103(a), which requires that the reference (or combination of references) disclose every element of the claim. As stated in the MPEP, "the prior art references (or references when combined) must teach or suggest all the claim limitations." MPEP § 706.02(j). Also, "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." MPEP 2143.01.

Claim 1 presently provides:

> 1. A method for reducing bus traversal in a media server comprising a host processor, a network interface, and a storage subsystem comprising one or more storage devices, the host processor and network interface being connected to a first input-output bus, the storage subsystem being connected to a second input-output bus, the first and second input-output buses being connected via a controller, the method comprising:
>
> **providing a hot-swappable adaptable cache connected to the first input-output bus, said adaptable cache comprising a data interface, core logic, and electronic storage media;**
>
> receiving a request for a media asset via a network, said request being received by the network interface;
>
> receiving the request at the adaptable cache;
>
> processing the request by the adaptable cache, wherein if the requested media asset is found on the electronic storage media, the media asset is

> returned to the user via the first bus and not the second bus, and wherein if the requested media asset is not found on the electronic storage media, the media asset is accessed from the storage subsystem and returned to the user via the second bus and first bus.

(emphasis added). The above limitation or close variations thereof is present in the remaining claims 2-23 by virtue of either containing a similar limitation or depending from a claim that contains such a limitation. In this regard, independent claim 23 has been amended to clearly state that the hot-swappable adaptable cache provided therein comprises a data interface, a core logic, and electronic storage media.

The combination of Asano and Olarig do not teach all the elements the above limitation for the following reason: the limitation requires the entire adaptable cache to be hot-swappable, not just the cache memory (electronic storage media) portion of the adaptable cache. As stated in the claim, the adaptable cache comprises **"a data interface, core logic, and electronic storage media".**

The official action combines the NIP of Asano (see official action page 4, lines 1-2) with the hot-plug cache memory of Olarig (official action page 5, lines 5-7) to allegedly arrive at the hot-swappable adaptable cache recited in the above limitation. The problem with such combination is that while it could plausibly (for the sake of argument) be construed to result in a NIP *with* a hot-plug cache (assuming motivation to combine was adequately demonstrated), it does not result in a NIP that is hot-pluggable *as a whole.*

The references do not provide any suggestion or motivation to combine the elements as contemplated by the office action. Asano does not teach or suggest removing, unplugging, or otherwise disconnecting a NIP from the system disclosed therein. When describing the connection of the NIP, Asano provides only that "the NIP [is] connected by a standard bus such as PCI (Peripheral Component Interconnect) bus…it is also possible to connect the

processor 21, the NIP local memory 22, and the PCI bus 26 by an ASIC (Application Specific Integrated Circuit) called bridge chip." See Asano col. 5, lines 1-8.

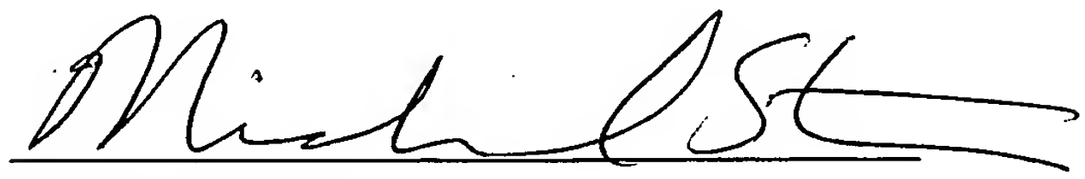
Olarig also fails to provide any suggestion or motivation to combine the elements as contemplated by the office action. While Olarig contemplates a hot-plug cache memory, it does not teach or suggest combining such a memory with additional components such as Asano's NIP components. Olarig discusses its cache memory modules in Fig. 2 and corresponding text at paragraphs 0047 and 0048. In paragraph 0047, Olarig states only that "cache memory modules 220 can be conventional cache memory modules."

For the reasons above, applicants believe that Asano, Olarig, and the other references of record are traversed.

Applicants respectfully request acknowledgment of the drawings filed on June 27, 2003 as formal.

Applicants respectfully request reconsideration of the outstanding rejection and await Examiner's action upon further review and consideration. Applicants' attorney, Nathaniel Ari Long, can be reached at 206-332-1380 to further discuss and resolve any outstanding issues relating to this application.

Date: February 8, 2006



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